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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/929,591	08/14/2001	Louis L. Hsu	728-216 (YOR9-2001-0444 U)	9143
7590	06/28/2005		EXAMINER	NGUYEN, DANNY
Paul J. Farrell, Esq. DILWORTH & BARRESE LLP 333 Earle Ovington Boulevard Uniondale, NY 11553			ART UNIT	PAPER NUMBER
			2836	

DATE MAILED: 06/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	09/929,591	HSU ET AL.	
	Examiner Danny Nguyen	Art Unit 2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 13 April 2005.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 2-6,8-11,13-16 and 18-22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 2-6,8-11,13-16 and 18-22 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 4/13/2005 have been fully considered but they are not persuasive.

Regarding the amended claims 10 and 20, applicant argued that Keeth does not teach the enable register is configured for isolating each of the plurality of macros from the external voltage supply. Examiner respectfully disagrees with the applicant's argument. Keeth discloses a memory device (DRAM) comprises a plurality of arrays (10). If one of the pluralities of arrays is found defect, it is independently electrically isolated from the remaining circuitry (col. 3, lines 19-30); and the memory device further comprises a programmable elements (such as register), which allow for isolating the defective arrays (col. 3, lines 58-64, and col. 9, lines 8-18). Thus, applicant's arguments with respect to claims 10 and 20 do not distinguish over the Keeth reference. However, Examiner agrees with applicant that both Keeth and Itoh do not teach the enable register which is coupled to the voltage limiter, the oscillator, and the charge pump enables or disables at least the limiter, the oscillator, and the pump. However, applicant's amendment necessitated the new ground(s) of rejection presented in this Office action.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

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invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 2-5, 9-11, 13-15, 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Keeth (USPN 5,946,257) in view of Kowalski (USPN 5,444,412).

Regarding claims 2, 8-11, 18-22, Keeth discloses an integrated circuit system (see fig. 1 and 8) having a plurality of macros (memory arrays 801(1) to 801(8)), the integrated circuit comprises an external voltage supply input (the external supply input voltage Vcc) configured to supply an external voltage to the integrated circuit; and a plurality of internal voltage supply generators (e.g. 804 (1) to 804 (8)), each connected to a respective macro and configured for receiving the external voltage for generating an internal voltage supply for operating its respective macro (e.g. col. 9, lines 55-60), and each of the plurality of internal voltage supply generators including at least one reference supply (such as 1004 shown fig. 10) for generating the voltage level, an enable register is configured for storing one of enable and disable signal for isolating each of the plurality of macros from the power supply (col. 3, lines 58-64, and col. 9, lines 8-18). Keeth does not disclose the generator, and feedback as claimed. Kowalski discloses a generator comprises a voltage limiter (e.g. voltage regulator in figure 2) for controlling the voltage level, an oscillator (col. 4, lines 54-57), a charge pump (such as charge pump PMP in figure 2), an enable register (such the logic circuit CL) for enabling or disabling at least the limiter, the oscillator, and the pump according the stored signal (col. 4, lines 18-35), and a feedback (VHT) from the pump to the limiter. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the generator device of Keeth to incorporate enable register which

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couples to the voltage limiter, an oscillator, and a charge pump and feedback signal as disclosed by Kowalski in order to provide a stable operating voltage level in memory device.

Regarding claim 3, Keeth discloses the external voltage is greater than the internal voltage (the internal supply voltage is approximately one half of the external supply voltage Vcc, see col. 9, lines 9, line 58).

Regarding claims 4, 13, 21, Keeth discloses a scan-chain formed by a chain of scannable register latches storing fuse information and switch enable/disable signal (see col. 4, lines 53-57).

Regarding claims 5, 14, 15, Keeth discloses each of the plurality of internal voltage generators comprises a reference voltage generator (1004) for generating and providing a reference voltage for driving at least one voltage generator (see fig. 10).

3. Claims 6, 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Keeth in view of Kowalski, and Hsu et al (USPN 6,343,044). Keeth and Kowalski disclose all limitations of claims 1 and 20 as discussed above, but do not disclose a substrate bias level generator, a negative word line level voltage generator, and a boosted high level voltage generator. Hsu discloses a memory (e.g. fig. 3) comprises a substrate bias level generator (Vbb), a negative word line level voltage generator (Vwl), and a boosted high level voltage generator (Vpp) (see col. 1, lines 10-42 and col. 5, lines 45-46). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the system of Keeth and Kowalski to incorporate a

Vbb generator, a Vwl generator, and a Vpp generator as taught by Hsuan in order to reduce cell leakage and improve the retention time (e.g. col. 1, lines 15-16).

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Danny Nguyen whose telephone number is (571)-272-2054. The examiner can normally be reached on Mon to Fri 8:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571)-272-2058. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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6/24/2005



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